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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/007,472	11/08/2001	Richard P. Mackey	42390P12248	3598

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EXAMINER	
HUYNH, KIM T	
ART UNIT	**PAPER NUMBER**
2112	

DATE MAILED: 03/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/007,472	MACKEY ET AL.	
	Examiner	Art Unit	
	Kim T. Huynh	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/23/05*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-29 are rejected under 35 U.S.C. 102(e) as being anticipated by Pawlowski et al. (Pub. No US20010037426)

As per claim 1. Pawlowski discloses a system comprising:

- a controller responsive to interrupt signals received on one or more interrupt signal inputs; [0025],[0034]
- an interrupt message receiver coupled to the one or more interrupt signal inputs; and [0042]
- a plurality of interrupt sources to transmit interrupt messages to the interrupt message receiver through a data bus; and [0032-0034]
- a register of bits each interrupt source corresponding with one bit, wherein the interrupt message receiver further comprises logic to initiate interrupt signals on the one or more interrupt signal inputs in response to receipt of interrupt messages from the data bus. ([0032-0034], ie, a vector is a descriptor that indicates to the target processor the I/O device in system

that is the source of the interrupt and every interrupt encoded within the message a corresponding bit in the pend_int register is asserted)

As per claims 9, 16, 23, Pawlowski discloses a method comprising:

- receiving interrupt messages on a data bus from a plurality of interrupt sources; [0035-0036]
- setting a bit in a register of bits in response to receipt of an interrupt message from an interrupt source corresponding with the bit, each interrupt source corresponding with one bit in the register; and [0032-0034]
- selectively initiating interrupt signals to a controller on one or more interrupt signal inputs in response to each received interrupt message.[0039-0040]

As per claims 2, 10, 17, 24, Pawlowski discloses wherein the interrupt message receiver comprises logic to decode each interrupt message in response to receipt of one or more write transactions received from the data bus. [0033-0034]

As per claims 3, 11, 18, 25, Pawlowski discloses wherein the system further comprises a register of bits, each interrupt source corresponding with one bit, and wherein the interrupt message receiver further comprises logic to set a bit in the register of bits in response to receipt of an interrupt message from an interrupt source corresponding with the bit and wherein the controller comprises logic to clear the bit in response to completion of servicing an interrupt associated with the interrupt message. [0042],[0056]

As per claims 4, 12, 19, 26, Pawlowski discloses wherein the controller comprises a first interrupt signal input to receive an IRQ interrupt signal and a second interrupt signal input to receive a FIQ interrupt signal. [0032-0033]

As per claims 5,13, 20, 27, Pawlowski discloses wherein controller comprises logic to service interrupts in response to interrupt signals received on the one or more interrupt signal inputs the system further comprises an interrupt controller comprising:

- logic to maintain a record of at least one unserviced interrupt message received at the interrupt message receiver from an interrupt source; and [0032]
- logic to initiate an interrupt signal on an interrupt signal input in to service the unserviced interrupt message in response to completion of an interrupt service by the controller. [0056]

As per claims 6, 14, 21, 28, Pawlowski discloses wherein the interrupt controller further comprises:

- logic to define a priority for one or more interrupt sources; [0039]
- logic to maintain a queue of unserviced interrupt messages based upon the priority; and [0039-0040]
- logic to select an unserviced interrupt message from the queue in response to completion of an interrupt service by the controller. [0056]

As per claims 7, 15, 22, 29, Pawlowski discloses wherein the interrupt controller further comprises a plurality of interrupt signal inputs and the interrupt controller further comprises:

- logic to associate each interrupt source with an interrupt signal input; [0033]
- logic to maintain a queue of unserviced interrupt messages for each interrupt signal input, each unserviced interrupt messages being received from an interrupt source associated with the interrupt signal input; and [0032]
- logic to select an unserviced interrupt message from a queue in response to completion of an interrupt service initiated at the interrupt signal input associated with the queue. [0056]

As per claims 8, Pawlowski discloses wherein the system comprises a plurality of controllers, each controller comprising one or more interrupt signal inputs, and wherein the interrupt message receiver is coupled to each interrupt signal input of the controllers.[0035-0036]

Response to Amendment

3. Applicant's amendment filed on 12/23/05 have been fully considered but are moot in view of the new ground(s) of rejection.

a. In response to applicant's argument that Pawlowski fails to disclose or suggest a register of bits, each interrupt source corresponding with one bit. Examiner respectfully disagrees. As Pwalowski notes at paragraphs 33-35, discloses the interrupt

handling system comprises an arrangement of interrupt queues and registers that enable the delivery of vectors to the appropriate processor or processors servicing the device interrupts. A vector is a descriptor that indicates to the target processor the I/O device in system that is the source of the interrupt. For example in response to signals issued by I/O device over the bus, the intermediary device encodes a message indicating that a particular interrupt has been asserted on the bus. In response to the encoded message, the PCA asserts a bit in the pend_int register corresponding to that interrupt. Thus for every interrupt encoded within the message a corresponding bit in the pend_int register is asserted. Thus, the prior art teaches the invention as claimed and the amended claims do not distinguish over the prior art as applied.

Conclusion

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

5. *Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kim Huynh whose telephone number is (571)272-3635 or via e-mail addressed to [kim.huynh3@uspto.gov]. The examiner can normally be reached on M-F 9.00AM- 6:00PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached at (571)272-3676 or via e-mail addressed to [rehana.perveen@uspto.gov].*

The fax phone numbers for the organization where this application or proceeding is assigned are (571)273-8300 for regular communications and After Final communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571)272-2100.

Kim Huynh

March 2, 2006

REHANA PERVEEN
SUPERVISORY PATENT EXAMINER
3/6/06